REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Office Action of November 28, 2006. Applicants have amended independent Claims 12 and 23 as set out above. Applicants have also added new independent Claim 30 as set out above. Applicants respectfully submit that the pending independent claims and the claims that depend therefrom are patentable over the cited references for at least the reasons discussed herein.

The Section 102 Rejections

Claims 12-19 stand rejected under 35 U.S.C. § 102 as being anticipated by United States Patent No. 5,583,362 to Maegawa (hereinafter "Maegawa"). *See* Office Action, page 2. Applicants respectfully submit that many of the recitations of these claims are neither disclosed nor suggested by the cited references. For example, amended Claim 12 recites:

> A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:
>
> forming a MOS transistor on an integrated circuit substrate, the MOS transistor having a source region, a drain region and a gate, the gate being between the source region and the drain region; and
>
> **forming a horizontal channel between the source and drain regions, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns, wherein the source and drain regions are formed in other patterns adjacent to sides of the spaced apart patterns**.

Applicants respectfully submit that at least the highlighted recitations of amended Claim 12 are neither disclosed nor suggested by Maegawa for at least the reasons discussed herein.

In particular, the Office Action points to layer 3 of Figure 15 of Maegawa as teaching the channel region as recited in Claim 12 of the present application. As discussed in the Abstract of Maegawa:

> A semiconductor device having at least one transistor having a channel member spaced from a semiconductor substrate, an insulating film on the substrate, and a control electrode on the channel member covering the channel member. **The control electrode forms a channel in each of two opposed surfaces of the channel member**. The channel member is a polycrystalline semiconductor.

See Maegawa, Abstract (emphasis added). Thus, referring to Figure 15 of Maegawa a channel is formed on both the upper and lower surfaces of the channel silicon film 3.

In stark contrast, Claim 12 of the present application has been amended to recite that the horizontal channel includes "at least two horizontal channel regions formed in spaced apart patterns, wherein the source and drain regions are formed in other patterns adjacent to sides of the spaced apart patterns.". In other words, the at least two horizontal channel regions and the source and drain regions are formed in separate patterns, for example, epitaxial layers. Nothing in Maegawa discloses or suggests at least these recitations of amended independent Claim 12. In fact, Maegawa discloses forming the source and drain regions in the same pattern as the horizontal channel. Accordingly, Applicants respectfully submit that amended independent Claim 12 and the claims that depend therefrom are patentable over Maegawa for at least the reasons discussed herein.

The Section 103 Rejections

Claims 20-29 stand rejected under 35 U.S.C. § 103 as being unpatentable over Maegawa in further view of United States Patent No. 6,420,758 to Nakajima (hereinafter "Nakajima"). *See* Office Action, page 6. Applicants respectfully submit that many of the recitations of these claims are neither disclosed nor suggested by the cited references. For example, independent Claim 23 recites, in part:

> A method of fabricating a transistor comprising:
> forming a trench region on an integrated circuit substrate to define an active region;
> forming a stacked structure including at least one set of first epitaxial patterns and second epitaxial patterns on the active region;...
> growing a third epitaxial layer on sidewalls of at least one set of first and second epitaxial patterns;...
> selectively etching the first epitaxial patterns of the set of at least one first and second epitaxial patterns to form a horizontal channel region having a plurality of spaced apart channel layers...

Applicants respectfully submit that at least portions of Claim 23 set out above are neither disclosed nor suggested by the cited combination for at least the reasons discussed herein.

In particular, the Office Action points to Maegawa as teaching the "selectively etching" step of Claim 23. The cited portion of Maegawa discusses a first conductive pattern (channel pattern or gate pattern) having a space and second conductive pattern covering the first conductive pattern after forming a gate insulating layer. The channel patterns are formed by repeating the formation of the first and second conductive patterns. The process discussed in Maegawa may include a complicated alignment process due to the repeated formation of

multiple layers. In stark contrast. Claim 23 recites "selectively etching the first epitaxial patterns of the set of at least one first and second epitaxial patterns to form a horizontal channel region having a plurality of spaced apart channel layers." Nothing in Maegawa discloses or suggests selectively etching the first epitaxial layer to form the channel region as recited in independent Claim 23. Furthermore, nothing in Maegawa discloses or suggests forming a third epitaxial layer on sidewalls of the first and second eptaxial layers as recited in Claim 23. Accordingly, Applicants respectfully submit that independent Claim 23 and the claims that depend therefrom are patentable over the cited combination for at least the reasons discussed herein.

Furthermore, the Office Action cites to embodiment 1 of Maegawa as teaching the step of forming the trench as recited in Claim 23 and embodiment 16 of Maegawa as teaching the step of forming the stacked structure as recited in Claim 23. Maegawa recites "the transistor in Embodiment 15 has a channel silicon film formed of two layer 3a and 3b. However, further multiple layers of channel silicon film, e.g., three, four or more layers may be formed." Thus, Maegawa clearly recites that embodiment 16 is a modification of embodiment 15, not embodiment 1. The Office Action arbitrarily combines the embodiments of Maegawa to teach the recitations of Claim 23 without any motivation besides Applicants' disclosure, which is an inappropriate basis for combination. Accordingly, Applicants respectfully submit that independent Claim 23 and the claims that depend therefrom are patentable over the cited combination for at least these additional reasons discussed herein.

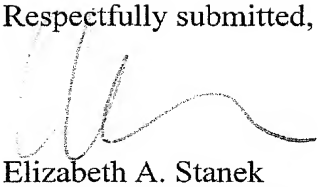
The New Claim is Patentable

Applicants have added new Claim 30 as set out above. Applicants respectfully submit that new Claim 30 is patentable over the cited references for at least the reasons discussed above with respect to Claim 12. Accordingly, Applicants respectfully submit that Claim 30 is in condition for allowance for at least the reasons discussed herein.

CONCLUSION

Applicants respectfully submit that pending claims are in condition for allowance for at least the reasons discussed herein, which is respectfully requested in due course. Favorable examination and allowance of the present application is respectfully requested.

Respectfully submitted,



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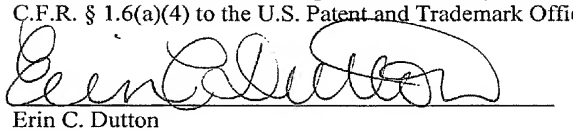

Erin C. Dutton